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17CS32

Third Semester B.E. Degree Examination, June/July 2019 Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

- 1 a. List any 4 differences between JFET and MOSFET. (04 Marks)
- b. Explain with help of neat diagram the working of N-channel JFET and sketch its characteristics. (08 Marks)
- c. With help of block diagram, explain the operation of a astable multivibrator using IC 555. (08 Marks)

OR

- 2 a. Sketch and explain the working of peak detector. (06 marks)
- b. State and explain any four performance parameters of an operational amplifier. (08 marks)
- c. Illustrate the various types of filters with neat diagram and definations. (06 Marks)

Module-2

- 3 a. Use a Karnaugh map to find minimum 80p form for the following Boolean function :
 $f(a, b, c, d) = \sum m(0, 2, 3, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$.
 Also draw the logic circuit diagram for the simplified SOP. (10 Marks)
- b. Apply Quine Mc-clusky method to find essential prime implicants for the Boolean function
 $f(a, b, c, d) = \sum m(1, 3, 6, 7, 10, 12, 13, 14, 15)$.
 Write prime implicant table. (10 Marks)

OR

- 4 a. There are 4 adjacent parking slots in Mega Inc. executive parking area. Each slot is equipped with sensor whose output is asserted high when a car is occupying the slot. Write a truth table so that the output is high if two or more vacant parking is available.
 - i) Write truth table
 - ii) Find the expression of the system that will signal the existence of two or more vacant slots
 - iii) Simplify the expression
 - iv) Draw the logic diagram for simplified expression. (10 Marks)
- b. Briefly explain an HDL implementation models. And write the HDL program for the following circuit shown in using in figure Fig.Q4(b) using structural model. (07 Marks)

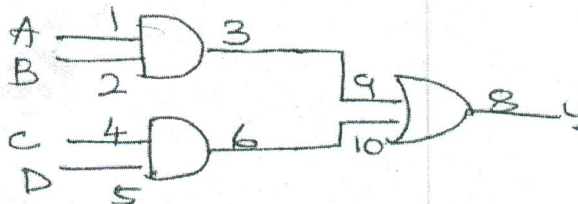


Fig.Q4(b)

- c. What is hazards? List the types of hazards. (03 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.



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Module-3

- 5 a. Implement the full adder outputs using 3 – 8 decoder. (07 marks)
b. Design one bit magnitude comparator and implement it using de-multiplexer (08 Marks)
c. Distinguish between combinational and sequential circuit. (05 Marks)

OR

- 6 a. Design a seven segment display using PLA. (10 Marks)
b. Show how 1 : 4 de-multiplexer is used to get 1 : 16 de-multiplexer. (04 Marks)
c. With the help of block diagram explain PAL and PLA. (06 Marks)

Module-4

- 7 a. The sequence 1011 is applied to the output of a 4 bit serial shift register that is initially cleared. With the help of diagram show how sequence is being entered serially into the register. (08 Marks)
b. Design a self correcting modulo-6 counter in which all the unused state leads to state ABC = 000. (08 Marks)
c. Draw the logic diagram, truth table and waveforms for a two flip-flop ripple counter. (04 Marks)

OR

- 8 a. Sketch a ring counter and Johnson counter and write its truth table. (08 Marks)
b. Explain how toggle flip-flop is used as frequency divider circuit. Sketch the output waveforms. (08 Marks)
c. A 4-bit binary asynchronous counter is connected. With a clock of 500 KHz frequency. Find the time period of the wave forms at the o/p of all the flop-flops. (04 Marks)

Module-5

- 9 a. Design synchronous counter for the sequence 1 – 3 – 5 – 7 – 1 using J-K flip-flop. (12 Marks)
b. Explain digital clock with neat diagram. (04 Marks)
c. Explain the terms accuracy and resolution for D/A converter. (04 Marks)

OR

- 10 a. Explain with block diagram the operation of successive approximation ADC. (08 Marks)
b. Explain the binary ladder with digital input 1100. (08 Marks)
c. For a 5 bit resistive divider, determine the following :
i) Weight assigned to binary
ii) Weight assigned to second and third LSB
iii) The change in output voltage due to a change in the LSB, the second LSB and the third LSB
iv) The output voltage for a digital input of 10101.
Assume 0 = 0V and 1 = +10V.
